FIG. 1
Prior Art

100

State	L0	L1	L2	L3	State	L0	L1	L2	L3
1	0	0	0	0	9	0	0	0	1
2	1	0	0	0	10	1	0	0	1
3	0	1	0	0	11	0	1	0	1
4	1	1	0	0	12	1	1	0	1
5	0	0	1	0	13	0	0	1	1
6	1	0	1	0	14	1	0	1	1
7	0	1	1	0	15	0	1	1	1
8	1	1	1	0	16	1	1	1	1

FIG. 1
Prior Art

100

State	L0	L1	L2	L3	State	L0	L1	L2	L3
1	0	0	0	0	9	0	0	0	1
2	1	0	0	0	10	1	0	0	1
3	0	1	0	0	11	0	1	0	1
4	1	1	0	0	12	1	1	0	1
5	0	0	1	0	13	0	0	1	1
6	1	0	1	0	14	1	0	1	1
7	0	1	1	0	15	0	1	1	1
8	1	1	1	0	16	1	1	1	1

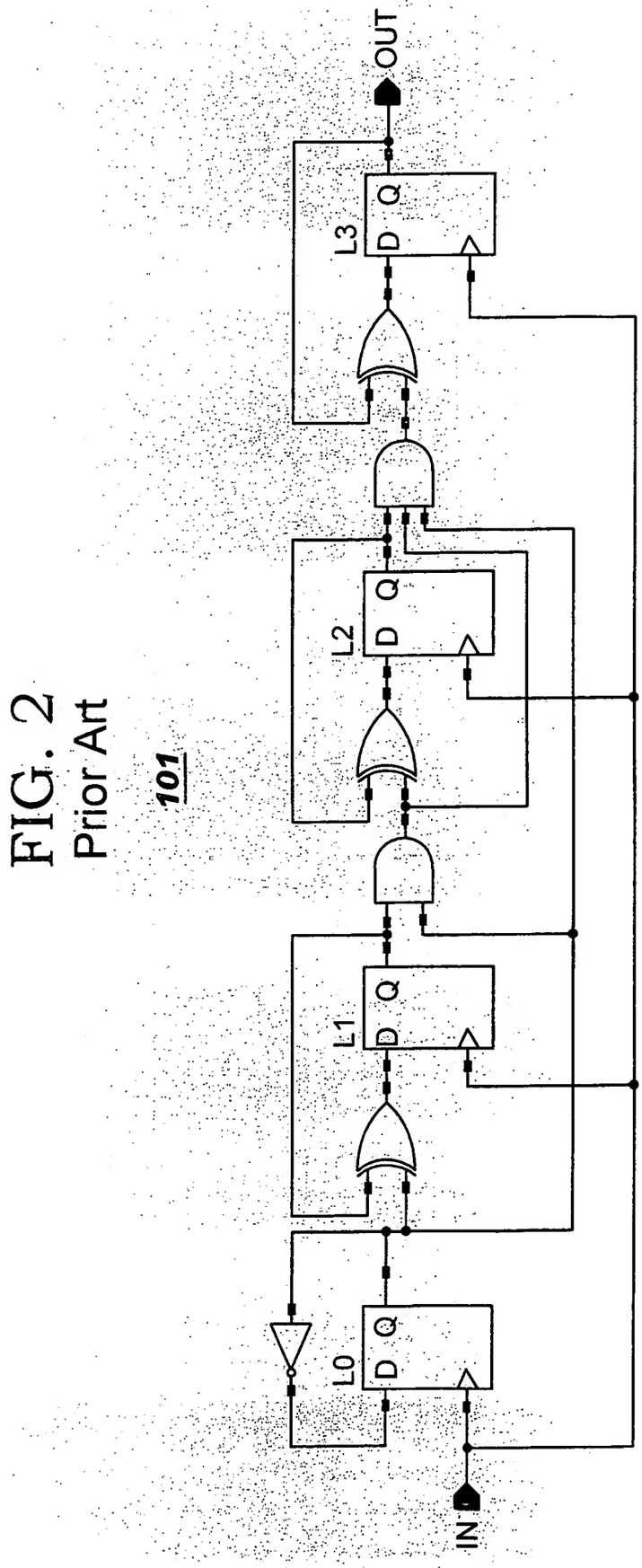


FIG. 2
Prior Art

101

FIG. 6
Prior Art

106

State	L0	L1	L2	L3	State	L0	L1	L2	L3
1	0	0	0	1	9	0	1	0	1
2	1	0	0	0	10	1	0	1	0
3	0	1	0	0	11	1	1	0	1
4	0	0	1	0	12	1	1	1	0
5	1	0	0	1	13	1	1	1	1
6	1	1	0	0	14	0	1	1	1
7	0	1	1	0	15	0	0	1	1
8	1	0	1	1					

FIG. 7

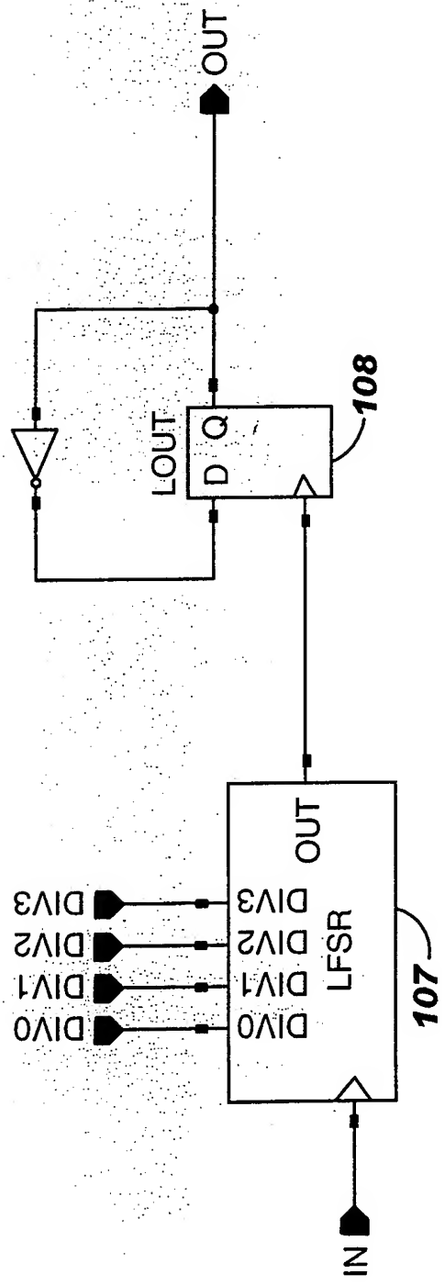


FIG. 8

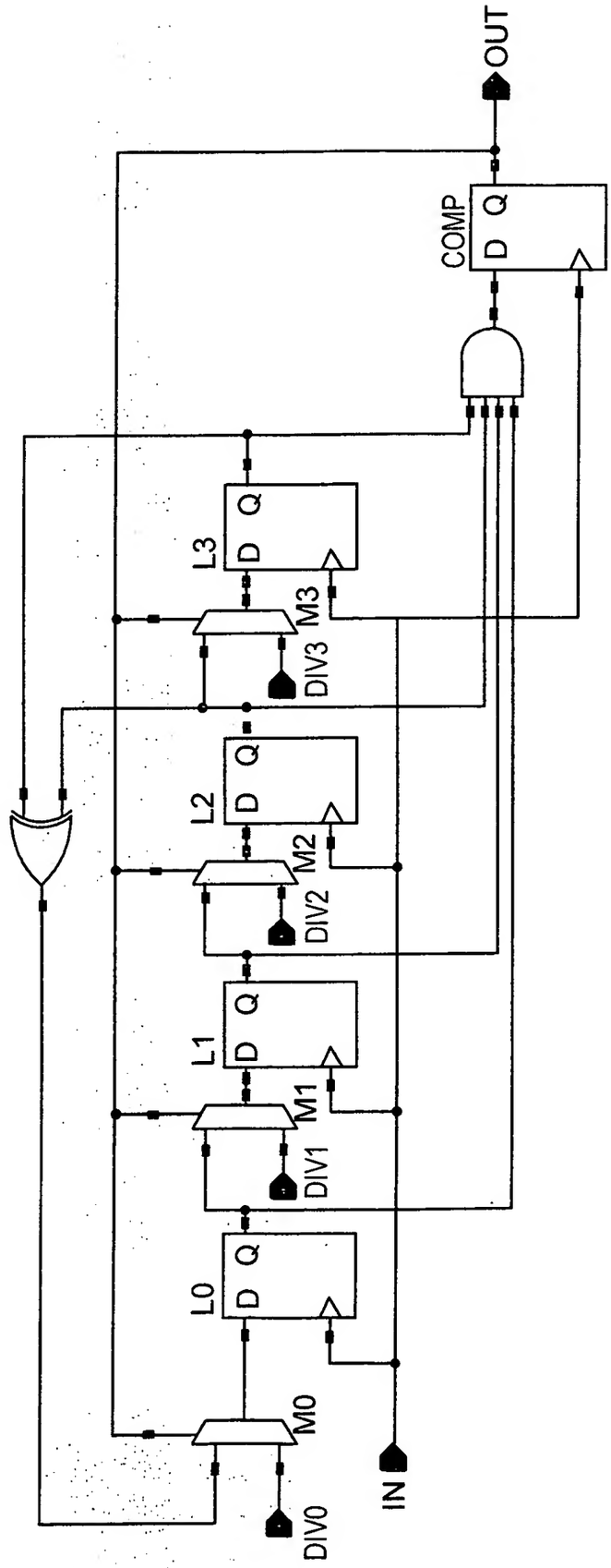


FIG. 9

LFSR Divide Value	DIV0	DIV1	DIV2	DIV3	LFSR Divide Value	DIV0	DIV1	DIV2	DIV3
1	0	0	0	0	9	1	1	0	0
2	1	1	1	1	10	1	0	0	1
3	1	1	1	0	11	0	0	1	0
4	1	1	0	1	12	0	1	0	0
5	1	0	1	0	13	1	0	0	0
6	0	1	0	1	14	0	0	0	1
7	1	0	1	1	15	0	0	1	1
8	0	1	1	0	16	0	1	1	1

FIG. 10

110

Final Divide Value	DIV0	DIV1	DIV2	DIV3	Final Divide Value	DIV0	DIV1	DIV2	DIV3
2	0	0	0	0	18	1	1	0	0
4	1	1	1	1	20	1	0	0	1
6	1	1	1	0	22	0	0	1	0
8	1	1	0	1	24	0	1	0	0
10	1	0	1	0	26	1	0	0	0
12	0	1	0	1	28	0	0	0	1
14	1	0	1	1	305	0	0	1	1
16	0	1	1	0	32	0	1	1	1

FIG. 11

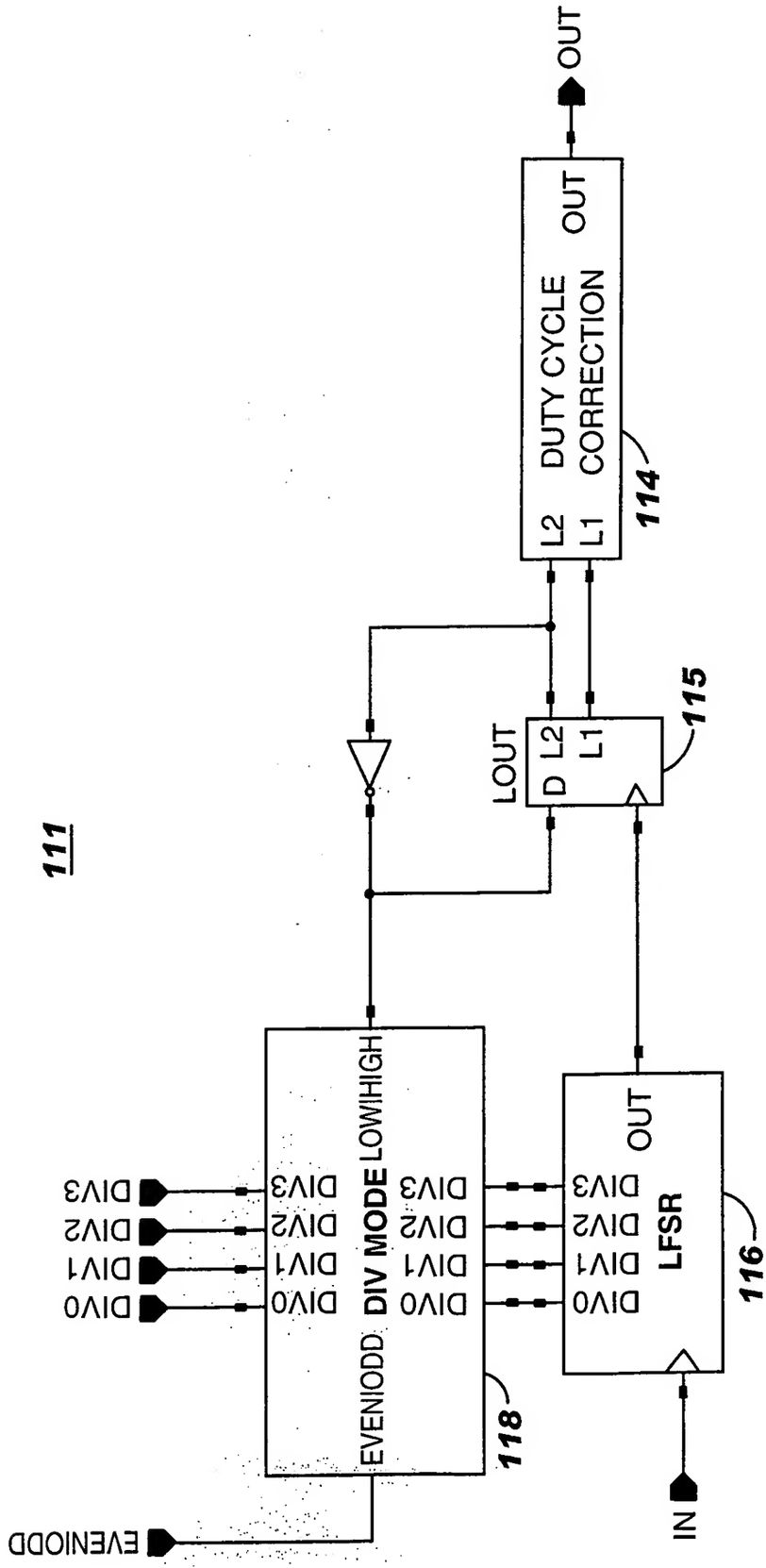
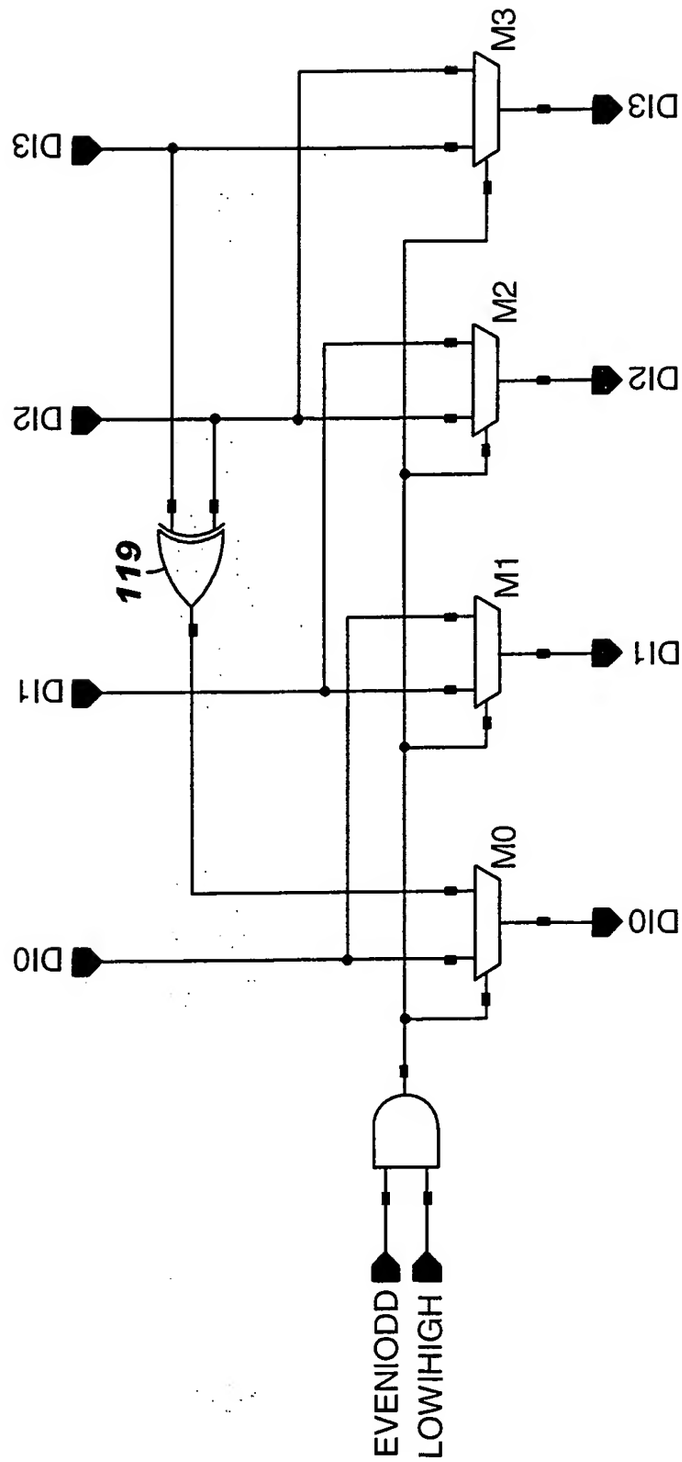

111
OUT
L2 DUTY CYCLE OUT
L1 CORRECTION
114
LOUT
D L2
L1
115
DIV3
DIV2
DIV1
DIV0
DIV MODE LOW|HIGH
EVENIODD
118
OUT
LFSR
116
IN
EVENIODD

FIG. 12

117

LFSR Divide Value	Final Divide Value	DIV0 'a'	LOW|HIGH=1 DIV1 'a'	DIV2 'a'	DIV3 'a'	LOW|HIGH=0 DIV0 'b'	DIV1 'b'	DIV2 'b'	DIV3 'b'
1	2	0	0	0	0	0	0	0	0
2,1	3	1	1	1	1	0	0	0	0
2	4	1	1	1	1	1	1	1	1
3,2	5	1	1	1	0	1	1	1	1
3	6	1	1	1	0	1	1	1	0
4,3	7	1	1	0	1	1	1	1	0
4	8	1	1	0	1	1	1	0	1
5,4	9	1	0	1	0	1	1	0	1
5	10	1	0	1	0	1	0	1	0

FIG. 13



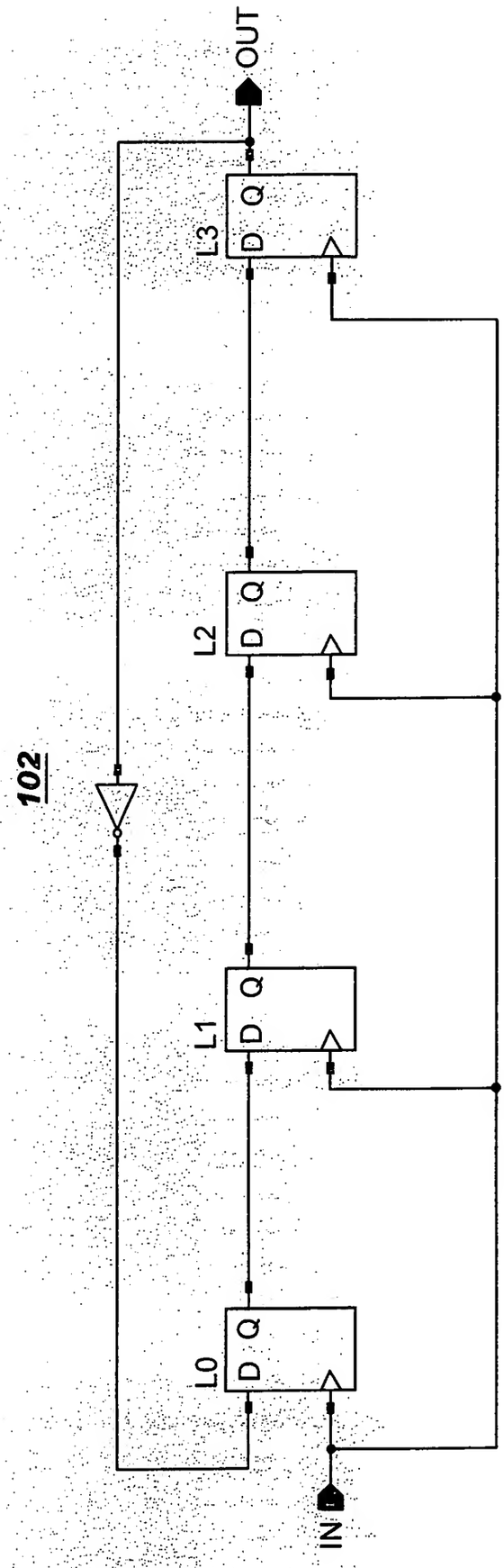


FIG. 3
Prior Art

FIG. 4
Prior Art

103

State	L0	L1	L2	L3	State	L0	L1	L2	L3
1a	0	0	0	0	1b	0	0	1	0
2a	1	0	0	0	2b	1	0	0	1
3a	1	1	0	0	3b	0	1	0	0
4a	1	1	1	0	4b	1	0	1	0
5a	1	1	1	1	5b	1	1	0	1
6a	0	1	1	1	6b	0	1	1	0
7a	0	0	1	1	7b	1	0	1	1
8a	0	0	0	1	8b	0	1	0	1

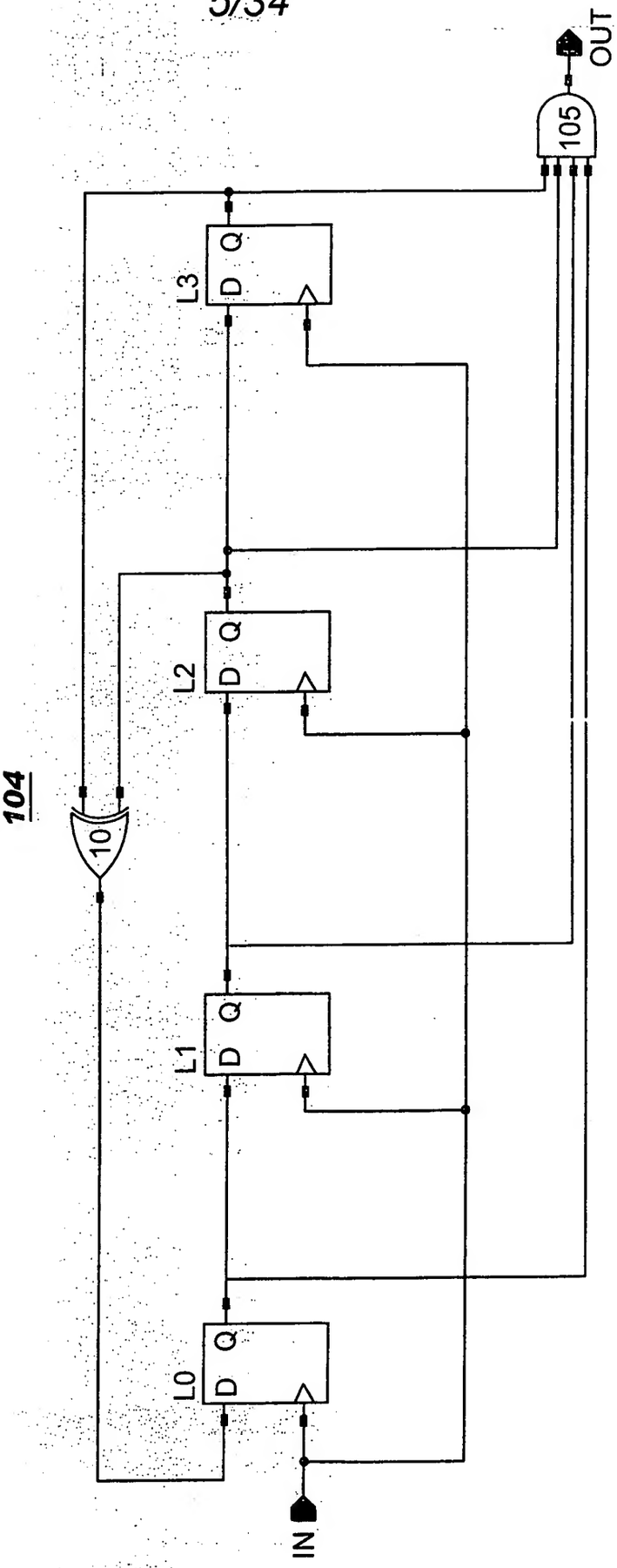


FIG. 5
Prior Art

FIG. 14

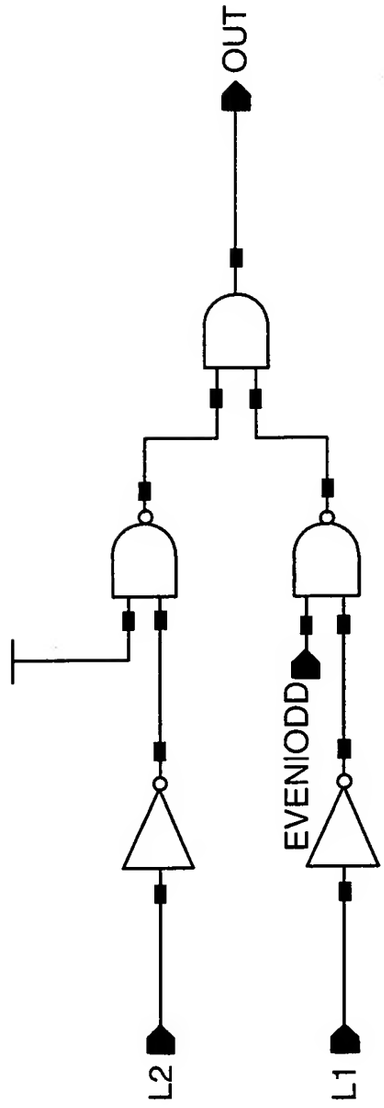


FIG. 15

Final Divide Value	DIV0	DIV1	DIV2	DIV3	DIV4	Final Divide Value	DIV0	DIV1	DIV2	DIV3	DIV4
1	0	0	0	0	1	17	1	1	0	0	1
2	0	0	0	0	0	18	1	1	0	0	0
3	1	1	1	1	1	19	1	0	0	1	1
4	1	1	1	1	0	20	1	0	0	1	0
5	1	1	1	0	1	21	0	0	1	0	1
6	1	1	1	0	0	22	0	0	1	0	0
7	1	1	0	1	1	23	0	1	0	0	1
8	1	1	0	1	0	24	0	1	0	0	0
9	1	0	1	0	1	25	1	0	0	0	1
10	1	0	1	0	0	26	1	0	0	0	0
11	0	1	0	1	1	27	0	0	0	1	1
12	0	1	0	1	0	28	0	0	0	1	0
13	1	0	1	1	1	29	0	0	1	1	1
14	1	0	1	1	0	30	0	0	1	1	0
15	0	1	1	0	1	31	0	1	1	1	1
16	0	1	1	0	0	32	0	1	1	1	0

FIG. 16

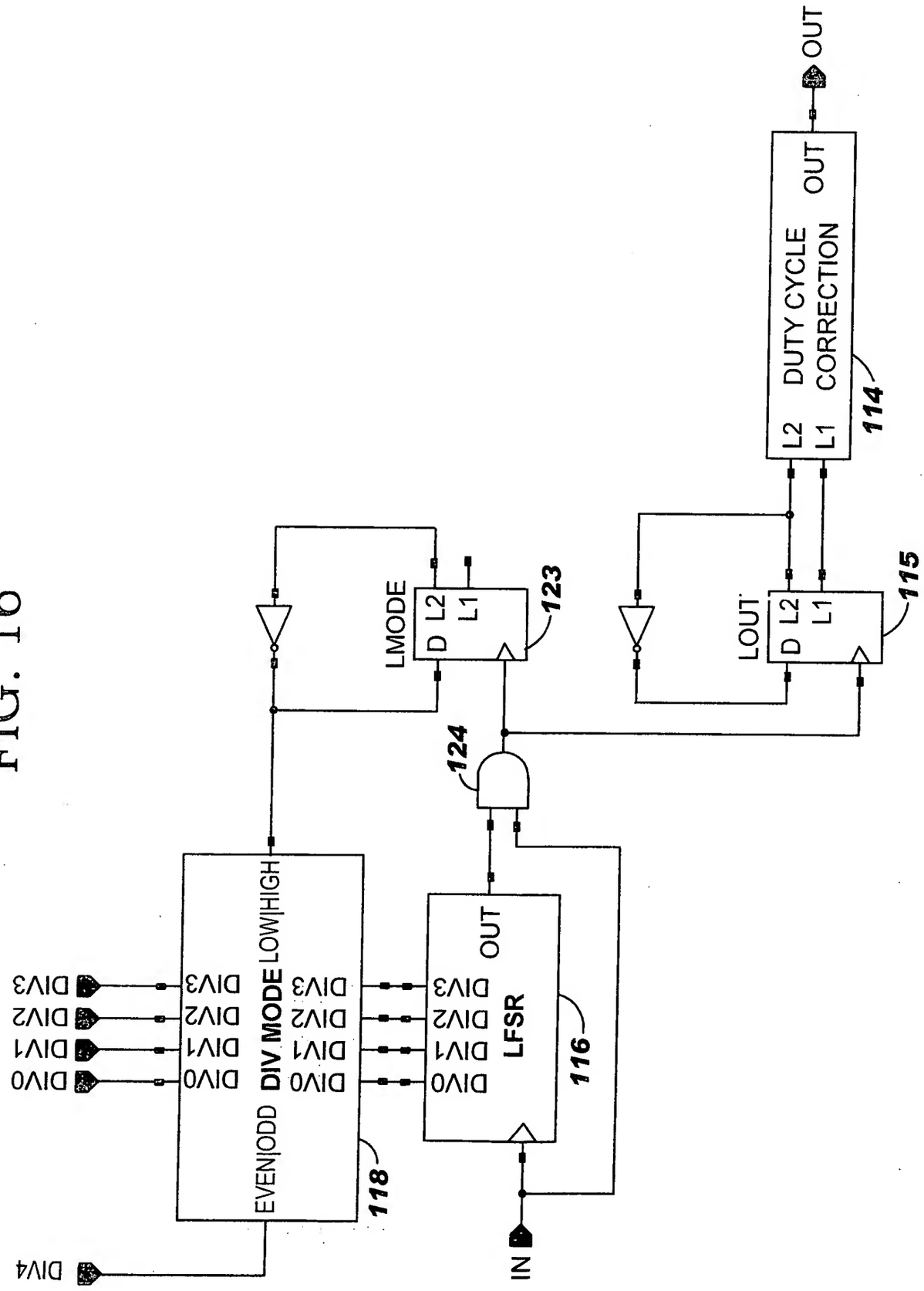

OUT
DUTY CYCLE CORRECTION
L2
L1
114
LMODE
D L2 L1
123
LOUT
D L2 L1
115
124
DIV3
DIV2
DIV1
DIV0
DIV MODE
LOW|HIGH
EVEN|ODD
118
DIV4
OUT
LFSR
116
IN

FIG. 17

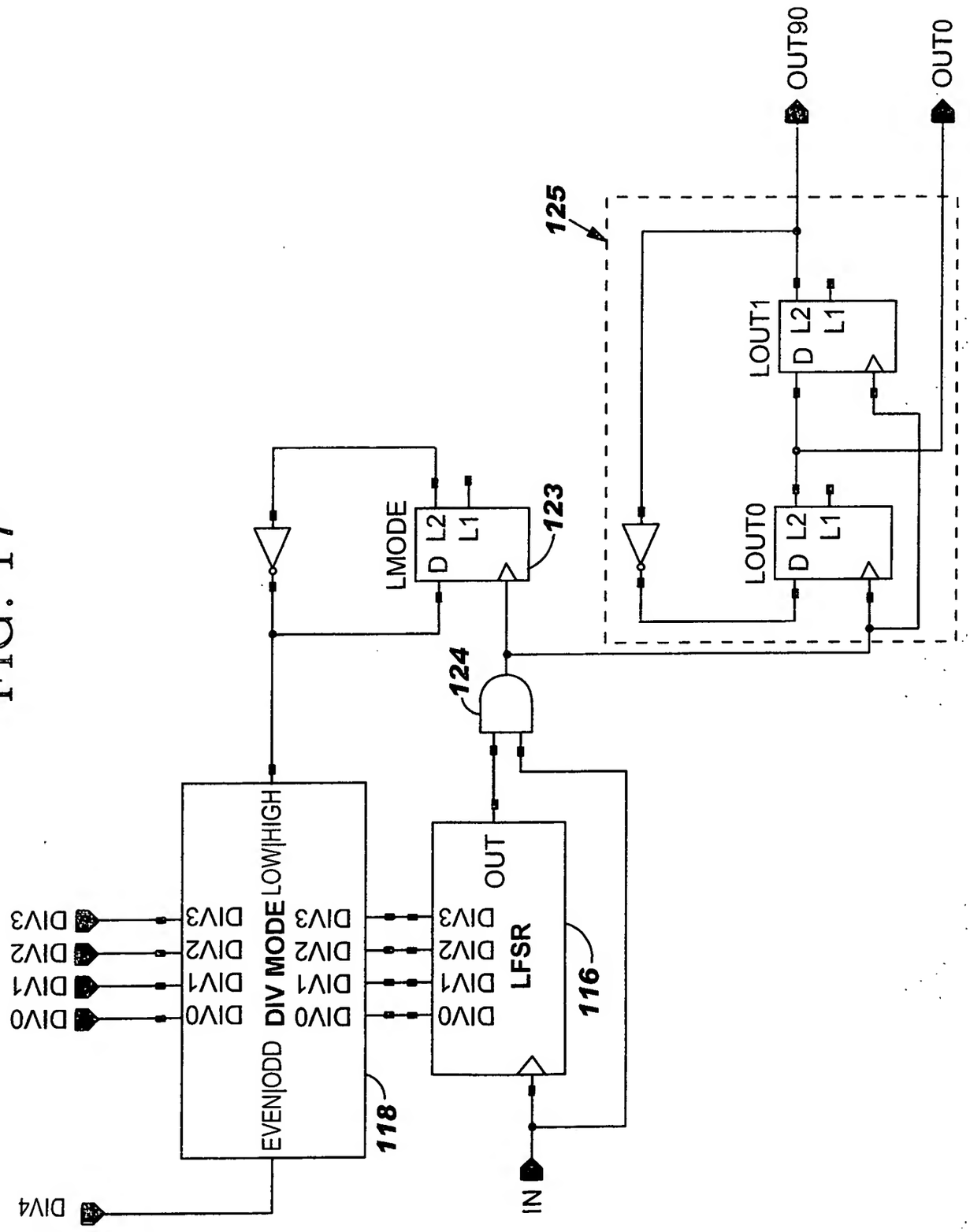

OUT90
OUT0
125
LOUT1
LOUT0
D L2 L1
LMODE
123
124
DIV4
DIV3
DIV2
DIV1
DIV0
EVEN|ODD
DIV MODE
LOW|HIGH
118
OUT
LFSR
116
IN

FIG. 18

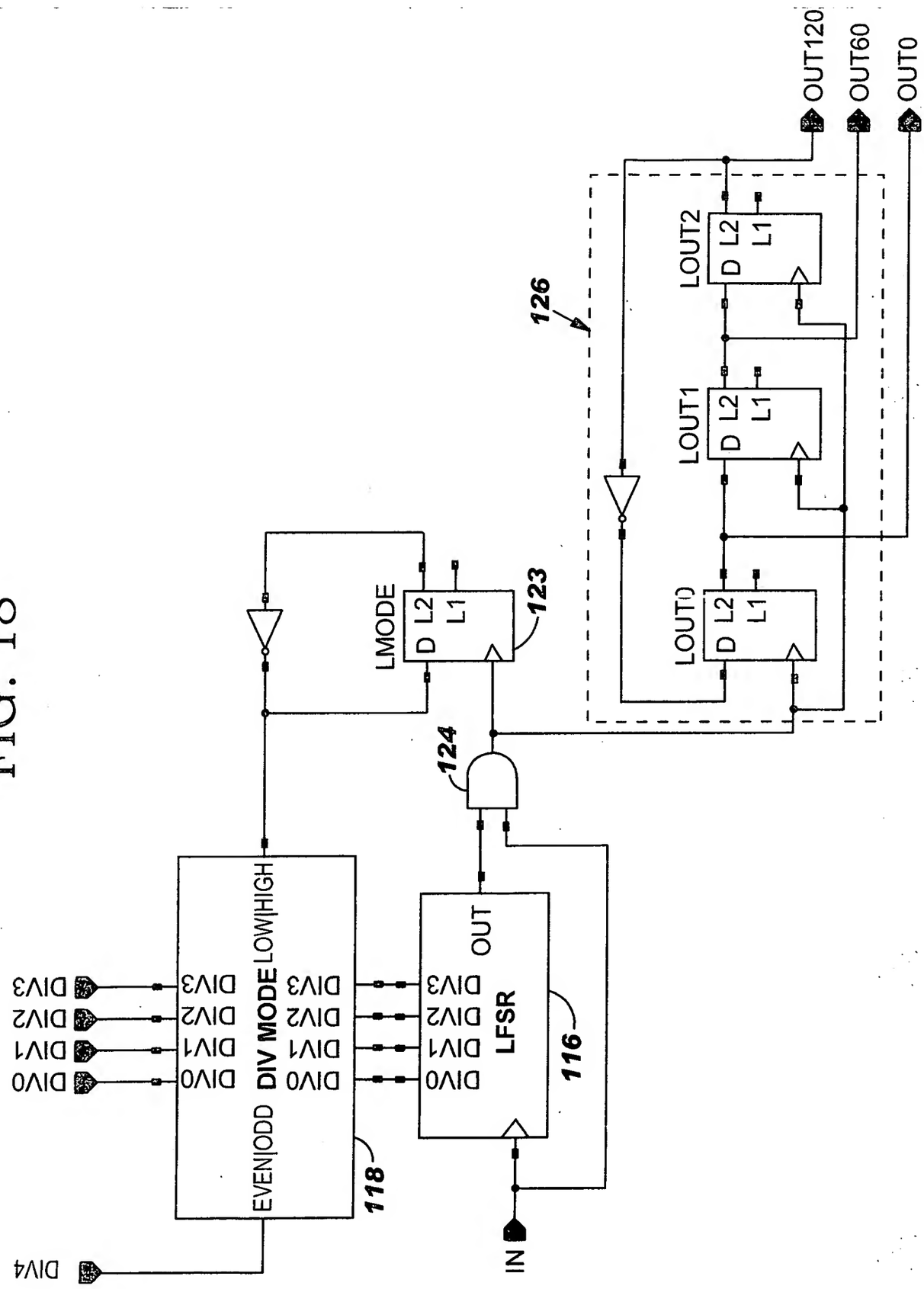

OUT120
OUT60
OUT0
126
LOUT2
LOUT1
LOUT0
D L2 L1
LMODE
123
124
DIV4
DIV3
DIV2
DIV1
DIV0
EVEN|ODD
DIV MODE
LOW|HIGH
118
OUT
LFSR
116
IN

FIG. 19

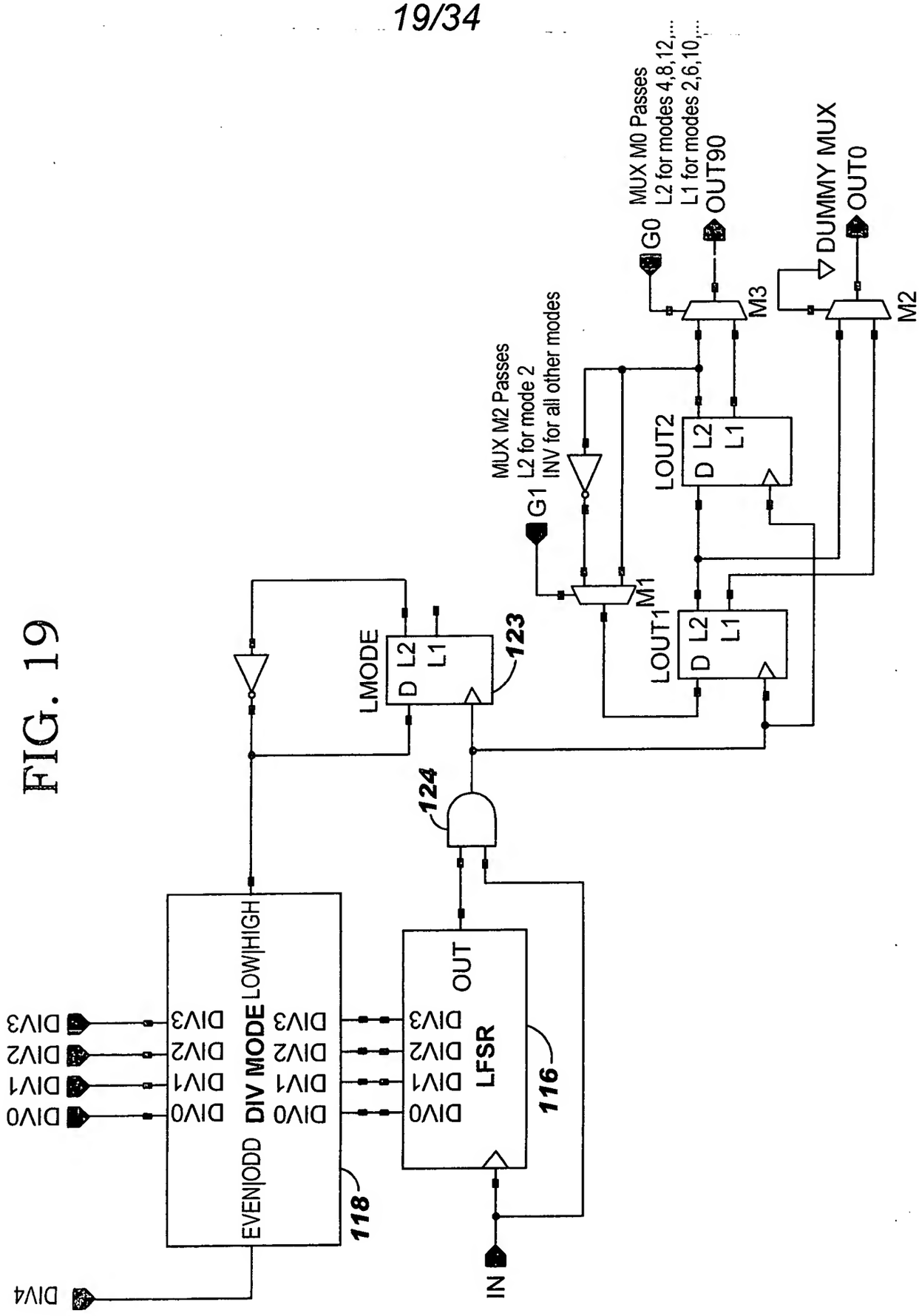

DIV4
DIV3
DIV2
DIV1
DIV0
EVEN|ODD
DIV MODE
LOW|HIGH
DIV3
DIV2
DIV1
DIV0
118
IN
DIV3
DIV2
DIV1
DIV0
LFSR
OUT
116
124
LMODE
D L2 L1
123
LOUT1
D L2 L1
LOUT2
D L2 L1
G1
MUX M2 Passes
L2 for mode 2
INV for all other modes
M1
G0
MUX M0 Passes
L2 for modes 4,8,12,...
L1 for modes 2,6,10,...
OUT90
M3
DUMMY MUX
OUT0
M2

FIG. 20

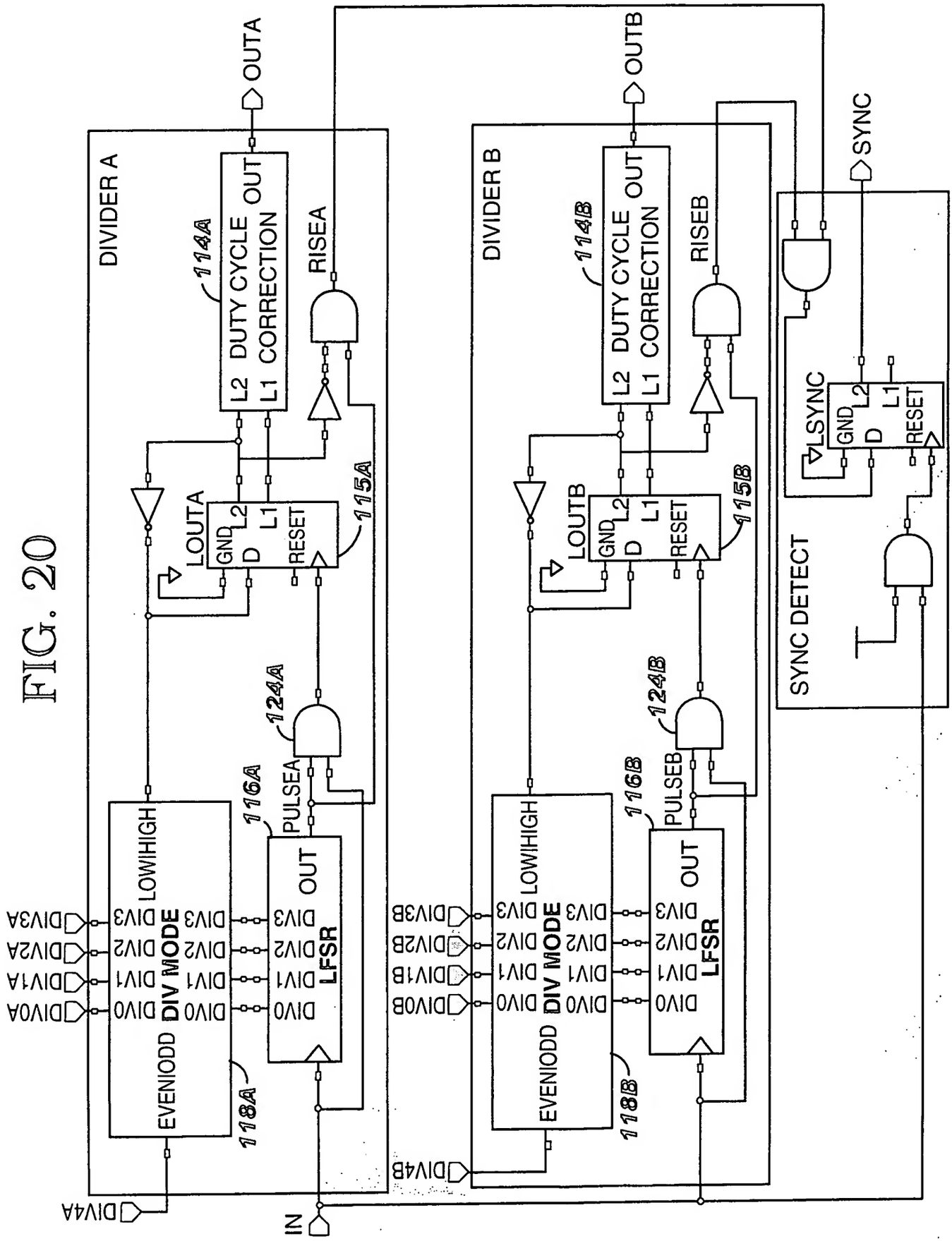

DIVIDER A
DIVIDER B
OUTA
OUTB
SYNC
114A
114B
L2 DUTY CYCLE CORRECTION OUT
L1
RISEA
RISEB
LOUTA
LOUTB
GND
D
L2
L1
RESET
115A
115B
LSYNC
SYNC DETECT
124A
124B
PULSEA
PULSEB
116A
116B
LOWIHIGH
DIV MODE
EVENIODD
LFSR
OUT
DIV0
DIV1
DIV2
DIV3
DIV0A
DIV1A
DIV2A
DIV3A
DIV0B
DIV1B
DIV2B
DIV3B
DIV4A
DIV4B
IN
118A
118B

FIG. 21

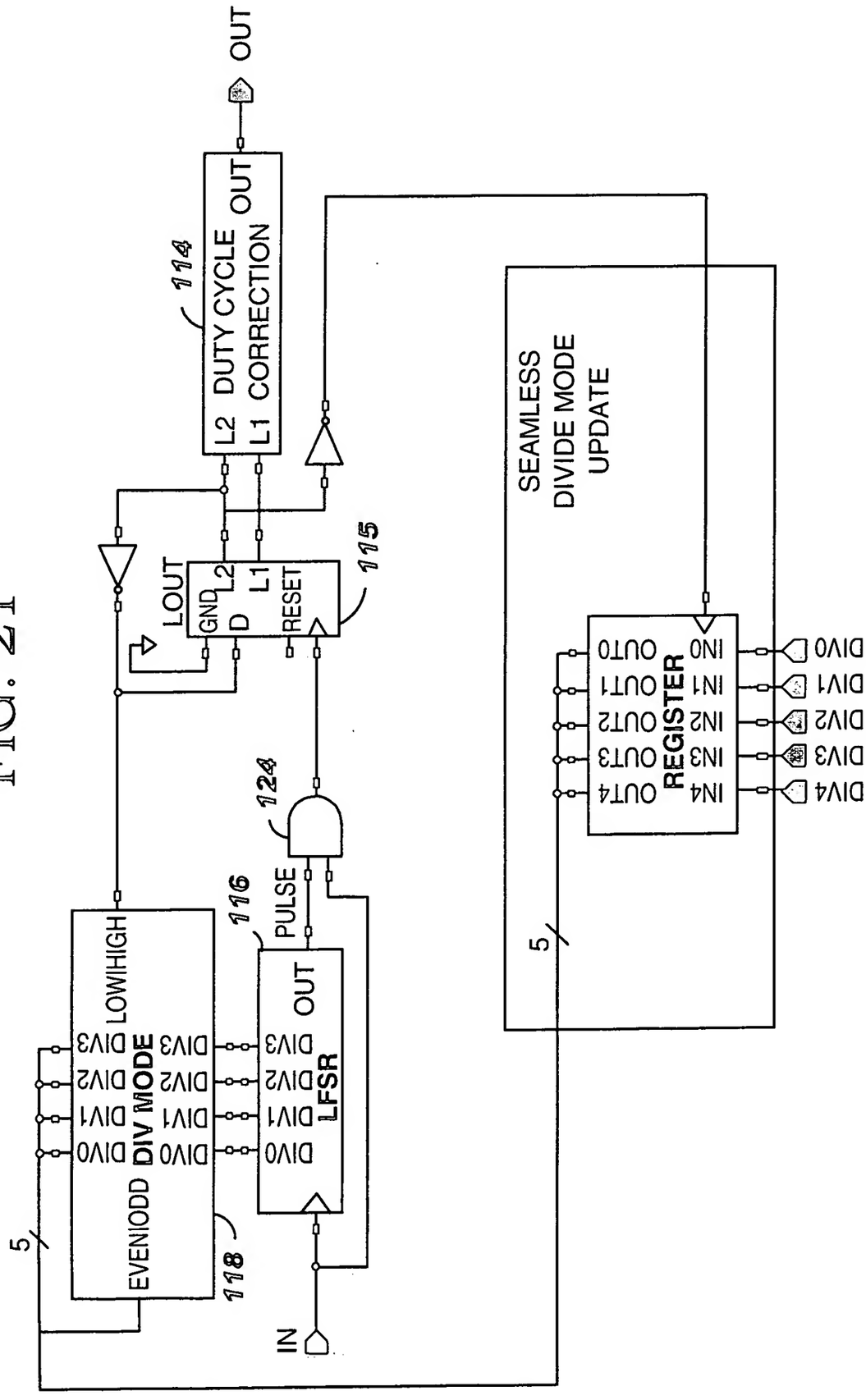

OUT
114
L2 DUTY CYCLE OUT
L1 CORRECTION
LOUT
GND
D
L2
L1
RESET
115
SEAMLESS
DIVIDE MODE
UPDATE
REGISTER
IN0
IN1
IN2
IN3
IN4
OUT0
OUT1
OUT2
OUT3
OUT4
DIV0
DIV1
DIV2
DIV3
DIV4
5
124
PULSE
116
OUT
LFSR
DIV0
DIV1
DIV2
DIV3
LOWIHIGH
DIV MODE
EVENIODD
118
IN

FIG. 22

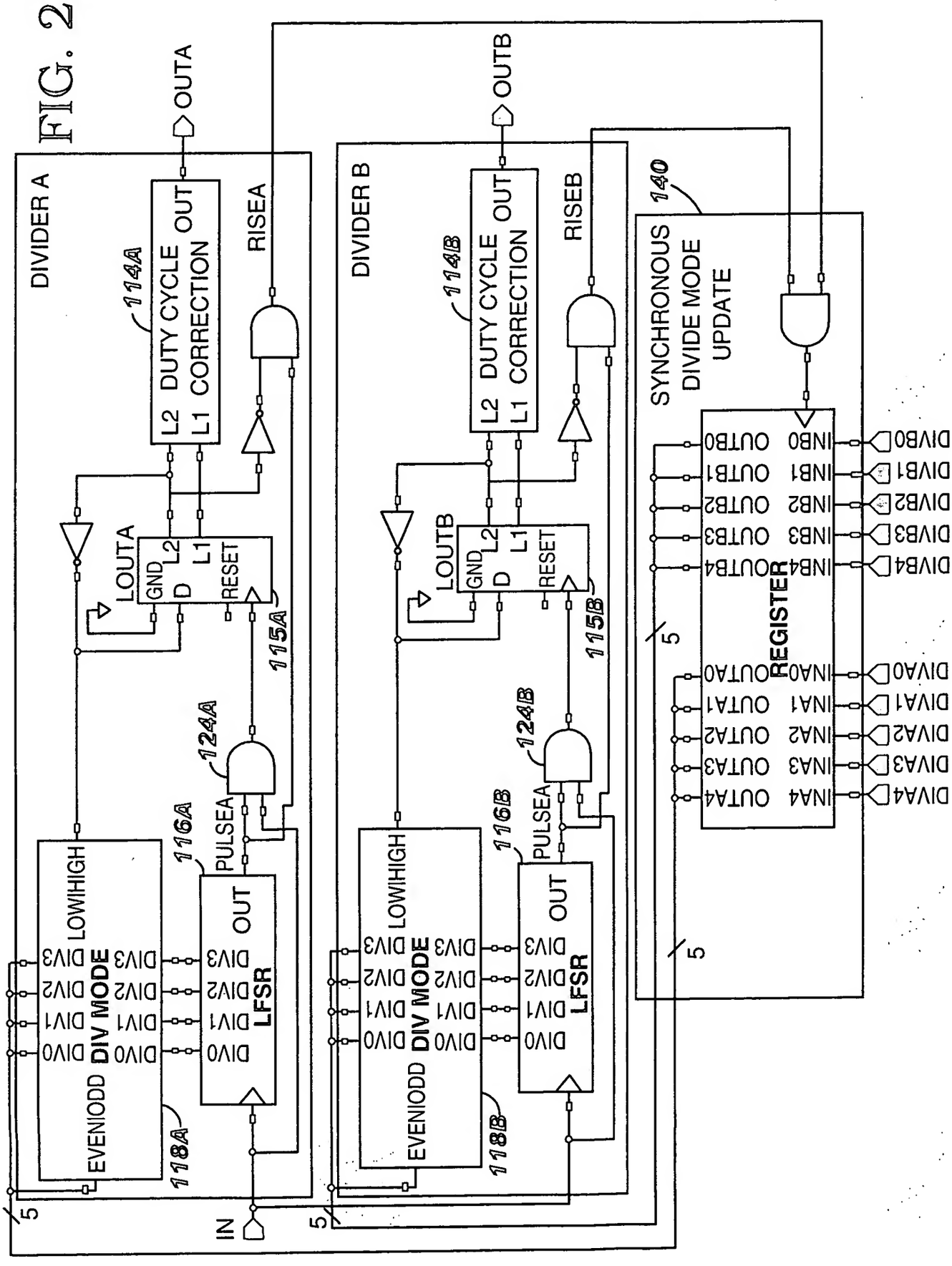

DIVIDER A
DIVIDER B
OUTA
OUTB
114A
114B
L2 DUTY CYCLE CORRECTION L1
OUT
RISEA
RISEB
LOUTA
LOUTB
GND D L2 L1 RESET
115A
115B
124A
124B
116A
116B
PULSEA
OUT
DIV3 DIV2 DIV1 DIV0 LFSR
LOWIHIGH
EVENIODD DIV MODE
118A
118B
IN
5
140
SYNCHRONOUS DIVIDE MODE UPDATE
REGISTER
INB0 INB1 INB2 INB3 INB4
OUTB0 OUTB1 OUTB2 OUTB3 OUTB4
INA0 INA1 INA2 INA3 INA4
OUTA0 OUTA1 OUTA2 OUTA3 OUTA4
DIVB0 DIVB1 DIVB2 DIVB3 DIVB4
DIVA0 DIVA1 DIVA2 DIVA3 DIVA4

FIG. 23

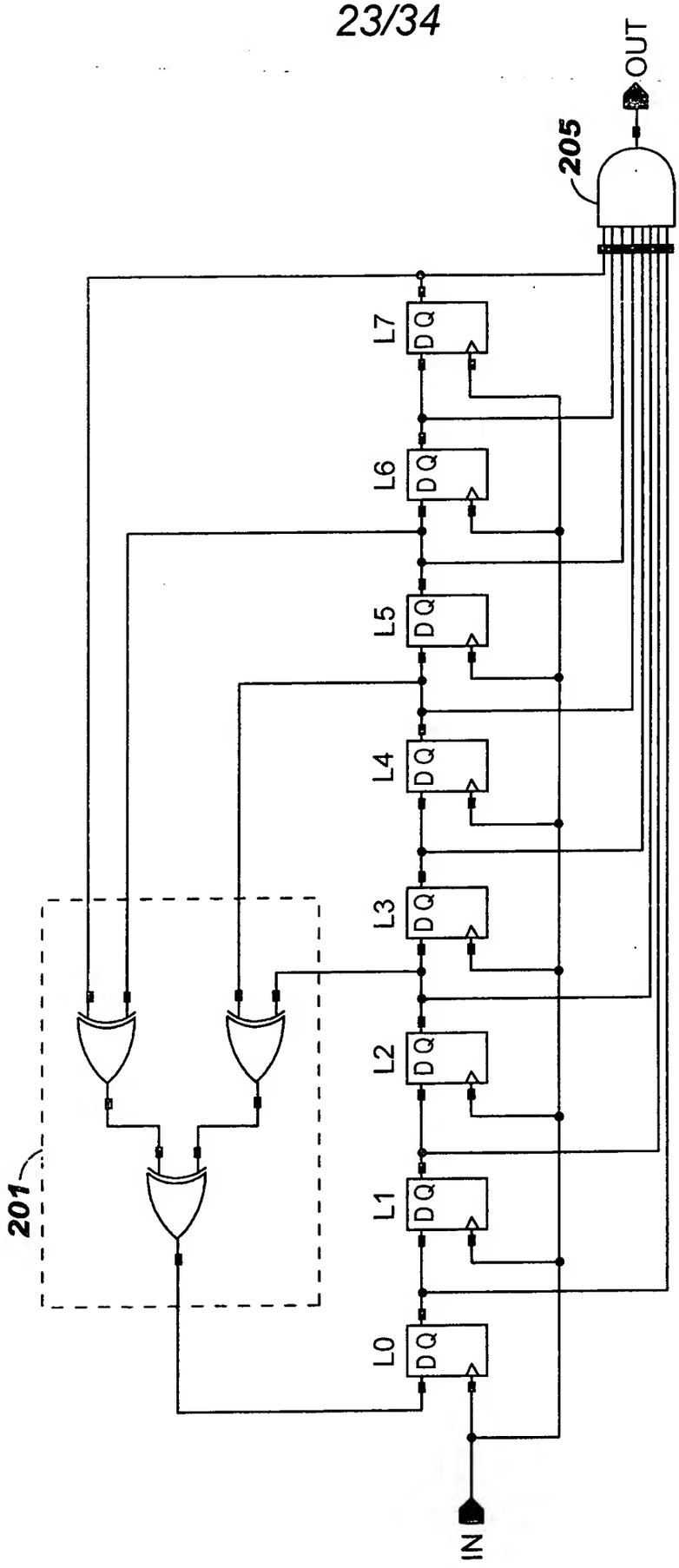


FIG. 24

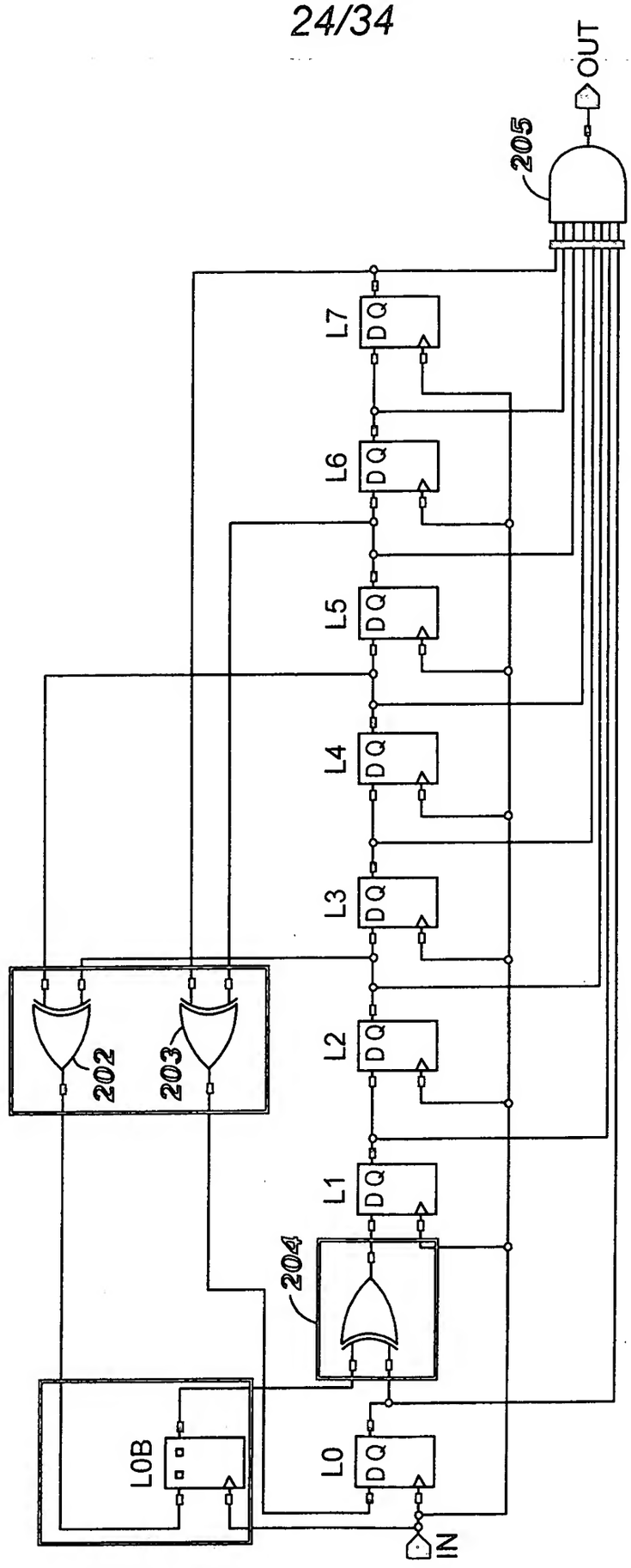


FIG. 25

L0	L1	L2	L3	L4	L5	L6	L7	State	Out
0	0	0	0	1	0	1	0	63	0
0	0	0	0	0	1	0	1	64	0
1	0	0	0	0	0	1	0	65	0
								66-->254	0
1	1	1	1	1	1	1	1	255(2^N-1)	1
0	1	1	1	1	1	1	1	1	0

FIG. 26

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L0	L1	L2	L3	L4	L5	L6	L7	State	Out
0	0	0	0	1	0	1	0	63	0
1	0	0	0	0	1	0	1	64	0
1	0	0	0	0	0	1	0	65	0

FIG. 27

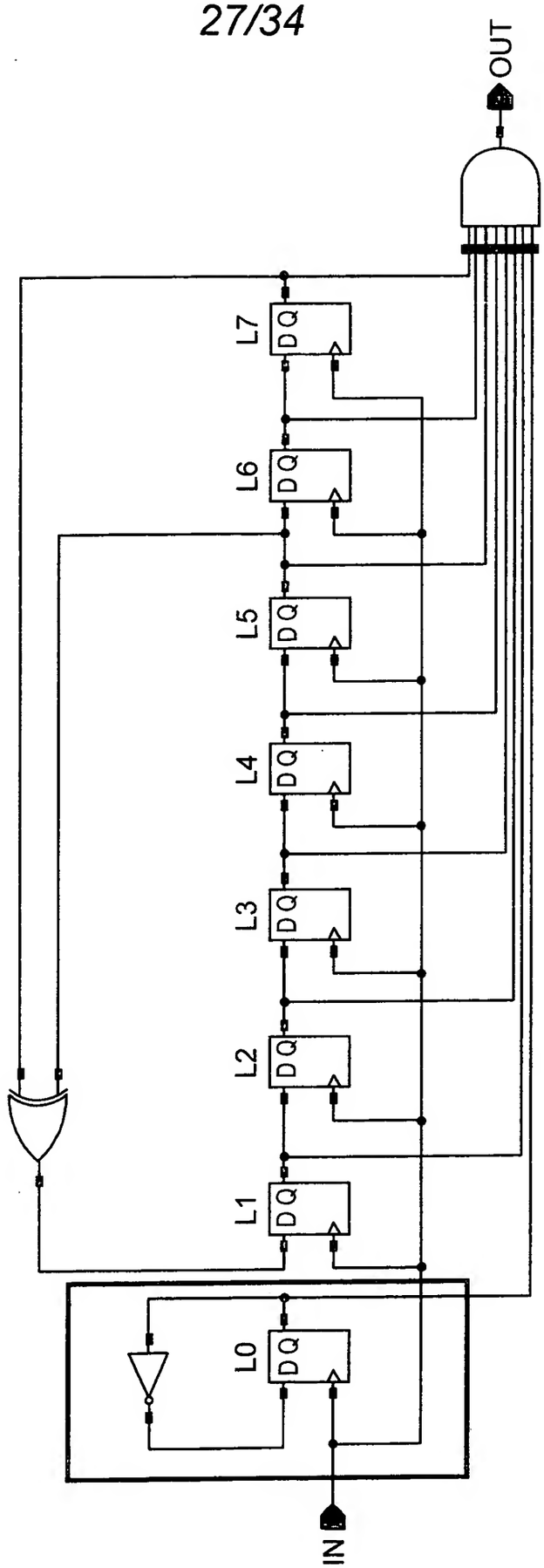

FIG. 28

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L0	L1	L2	State	Out
0	0	1	1	0
1	1	0	2	0
0	1	1	3	0
1	0	1	4	0
0	1	0	5	0
1	1	1	6 (2^N-2)	1
0	0	1	1	0
1	1	0	2	0
0	1	1	3	0

FIG. 29

220

L0	L1	L2	State	Out
0	0	0	1	0
1	0	1	2	0
0	1	0	3	0
1	1	1	4 [2(N-1)]	1
0	0	0	1	0
1	0	1	2	0
0	1	0	3	0

FIG. 30

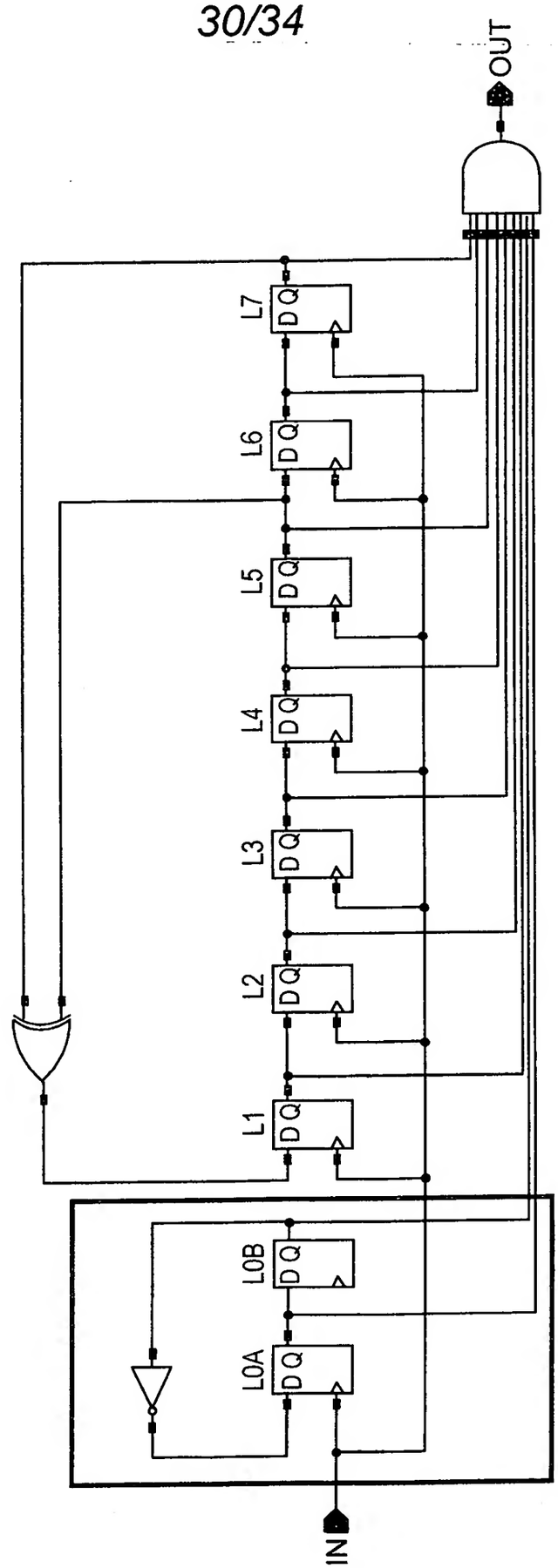

FIG. 31

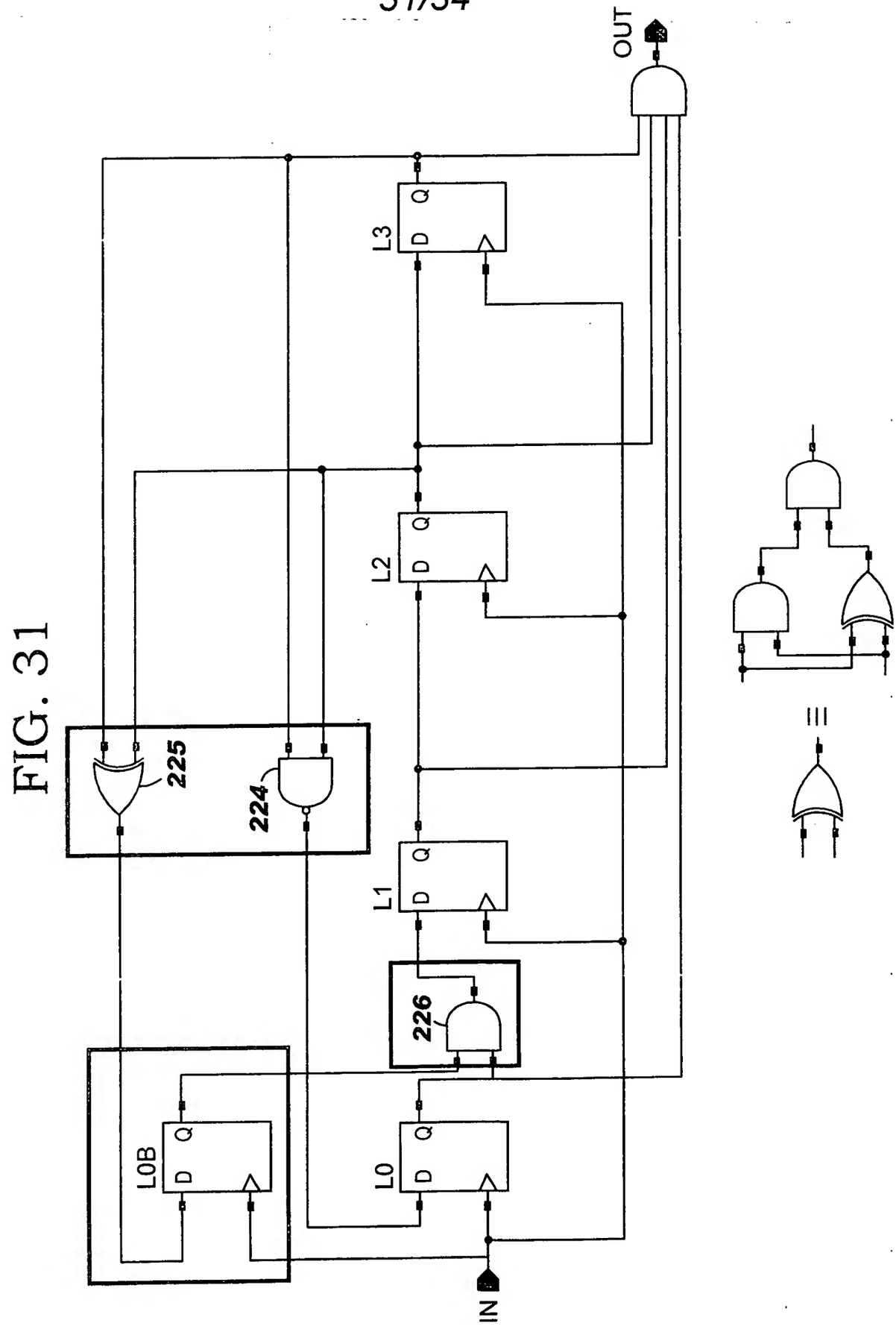

FIG. 32

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L0	L1	L2	L3	L0B	State	Out
0	1	1	1	0	1	0
0	0	1	1	0	2	0
0	0	0	1	0	3	0
1	0	0	0	0	4	0
1	1	0	0	1	5	0
1	0	1	0	1	6	0
1	0	0	1	0	7	0
1	1	0	0	0	8	0
1	1	1	0	1	9	0
1	0	1	1	0	10	0
0	1	0	1	0	11	0
1	0	1	0	0	12	0
1	1	0	1	0	13	0
1	1	1	0	0	14	1
1	1	1	1	0	15(2^N-1)	0
0	1	1	1	0	1	0
0	0	1	1	0	2...	

FIG. 33

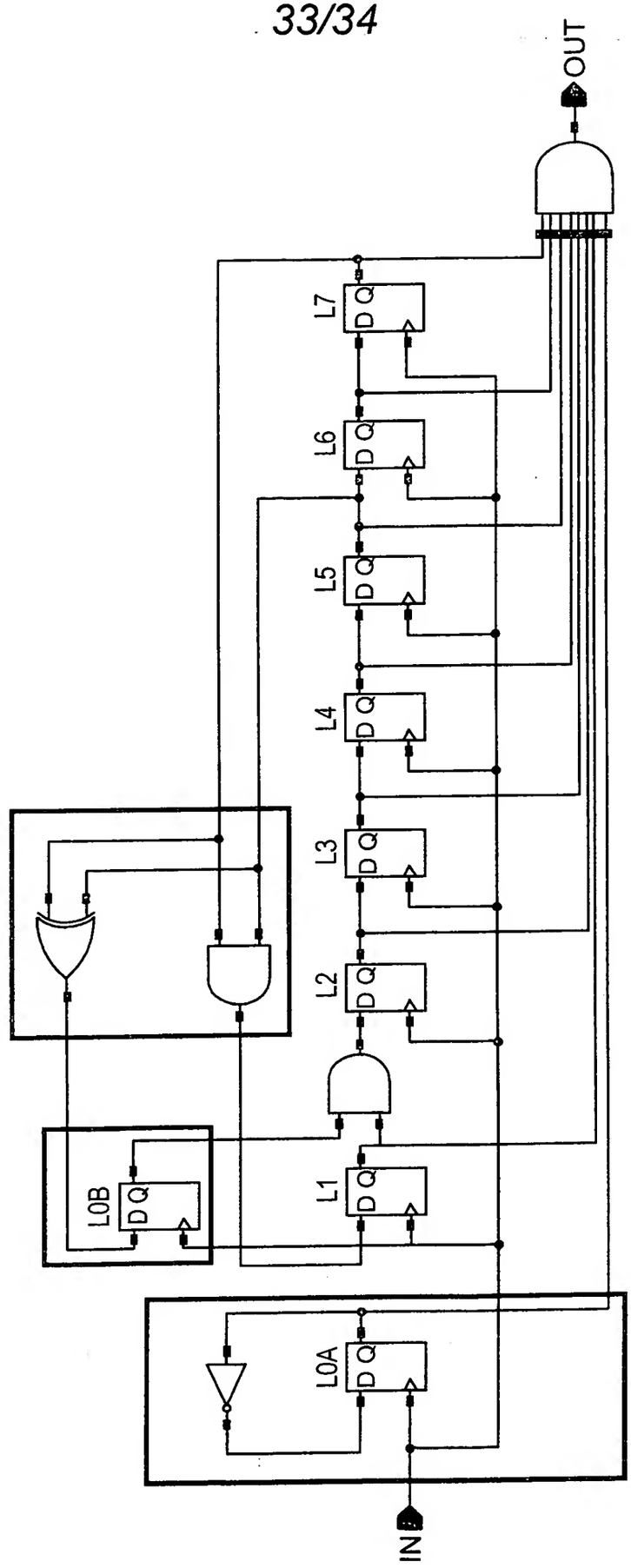
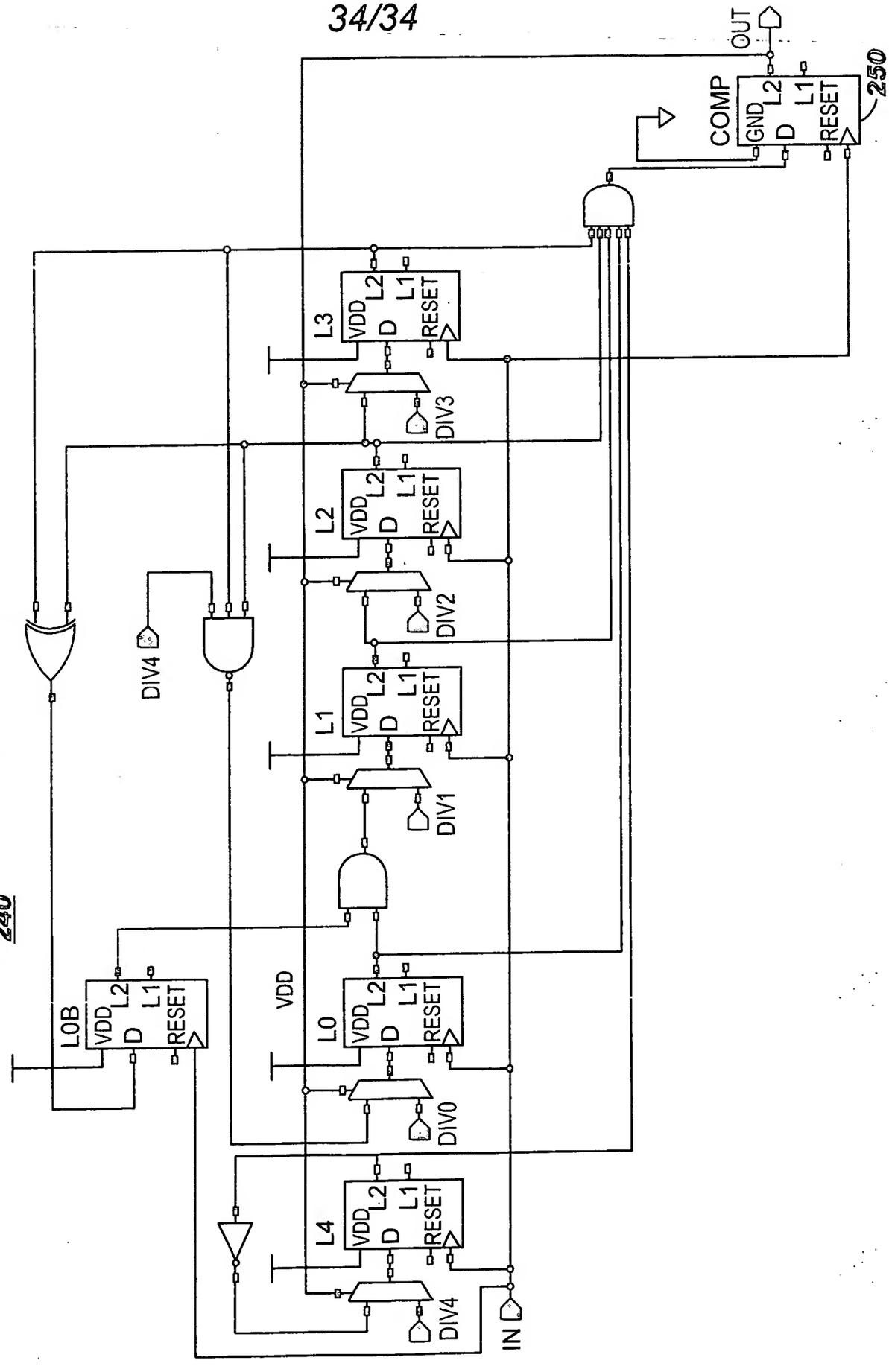


FIG. 34


240
250
OUT
COMP
GND
L2
L1
D
RESET
L3
VDD
DIV3
L2
DIV2
DIV4
L1
DIV1
L0B
L0
VDD
DIV0
L4
IN